THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HIROSHI TAKENO

Appeal No. 2006-1176
Application No. 09/926,202[1]

ON BRIEF

Before KIMLIN, PAK, and KRATZ, Administrative Patent Judges.

PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the examiner's refusal to allow claims 6 through 21 which are all the claims pending in the above-identified application. We have jurisdiction pursuant to 35 U.S.C. § 134.

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[1] Application for patent filed September 24, 2001.

APPEALED SUBJECT MATTER

The subject matter on appeal is directed to a process for forming an epitaxial semiconductor wafer having internal microdefects, without causing external microdefects in a device formation region (the vicinity of a top surface) of the wafer. See the specification, pages 1-4. The internal microdefects "work as gettering sites that capture heavy metal impurities and others by an action of a so-called internal gettering (IG)." See the specification, pages 1-2. Details of this process are recited in representative claims 6 and 10[2] which are reproduced below:

> 6. A manufacturing process for a silicon epitaxial wafer comprising the steps of:
> forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer; and
> applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C;
> thereby forming new oxygen precipitation nuclei and increasing bulk defect density, without reducing internal gettering.
>
> 10. The manufacturing process for a silicon epitaxial wafer according to claim 6, wherein a substrate resistivity of the epitaxial wafer is 0.02 Ω-cm or lower.

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[2] For purposes of this appeal, we limit our discussion to specifically argued claims 6 and 10 consistent with 37 CFR § 41.37(c)(1)(vii)(2004).

PRIOR ART REFERENCES

The prior art references relied upon by the examiner are:

Wijaranakula et al. (Wijaranakula) 5,418,855 Mar. 18, 1997

Wolf et al. (Wolf), *Silicon Processing for the VLSI Era*, Volume 1: Process Technology, Lattice Press, Sunset Beach, California, pp. 26-30 and 59-61, 124, 133-136 (1986).

REJECTION

Claims 6 through 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Wijaranakula and Wolf.

OPINION

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by the examiner and the appellant in support of their respective positions. This review has led us to conclude the examiner's Section 103 rejection is well founded. Accordingly, we affirm the examiner's Section 103 rejection for essentially the reasons set forth in the Brief and below. We add the following primarily for emphasis and completeness.

The examiner finds (the Answer, page 4), and the appellant does not dispute (the Brief, page 5) that Wijaranakula describes all the elements of the claimed invention, except for the claimed epitaxial layer deposition temperature and oxygen concentration

in units of atoms/cm^3. Indeed, Wijaranakula teaches at column 3, lines 4-21, that:

> In accordance with the invention, a semiconductor silicon crystal ingot containing sufficient dissolved oxygen, typically between 10 ppma and 50 ppma, is grown, preferably by using a Czochralski process. The ingot is then sliced into wafers, which are processed using known methods to produce a semiconductor silicon substrate having a polished surface. An epitaxial layer of a predetermined thickness is deposited onto the semiconductor silicon substrate to produce an epitaxial silicon wafer. The epitaxial silicon wafer then undergoes a first, or nucleation, annealing step, in which it is maintained for a first period of time within a first temperature range to form oxide microdefects in the silicon wafer substrate. The epitaxial layer, however, contains no nucleation sites or nuclei to form microdefects.
>
> The epitaxial silicon wafer then undergoes a second, or growth, annealing step, in which it is maintained at a second temperature for a second, typically extended period of time to grow or enlarge the microdefects.

Wijaranakula teaches that the deposition of an epitaxial layer is preferably carried out by chemical vapor deposition, see column 5, lines 6-9, and the first annealing step is preferably carried out at a temperature between 650° C and 750° C, see column 5, lines 33-48. According to Wijranakula (column 5, lines 41-44):

> The optimum temperature and duration within the above-described ranges are interrelated, depend upon the dissolved oxygen content of substrate 12, and can be determined by skilled persons.

To account for the epitaxial layer deposition temperature and oxygen concentration in units of atoms/cm^3 missing in Wijranakula, the examiner refers to the teachings of Wolf. We

find that Wolf teaches at page 59 that the oxygen content (10 ppma - 50 ppma) described in Wijranakula embraces the claimed oxygen content defined in units of atoms/cm^3. Specifically, Wolf teaches that "the most abundant impurity in Czochralski (CZ) Si crystal is oxygen, with concentrations typically ranging from $5X10^{17}$-$1X10^{18}$ atoms/cm^3 (or 10-20 ppma)." See page 59. We find that Wolf also teaches at pages 135 and 136, Figures 12, 13 and 14 that conventional epitaxial layer deposition temperatures include 1000° C and greater, which according to column 2, lines 1-7, of Wijaranakula "drive off oxygen near their surfaces..." We find that Wolf further teaches that:

> The growth rate of the epitaxial film depends on several parameters: a)chemical source; b) deposition temperature and c) mole fraction of reactants.

Given the above teachings, we concur with the examiner that the employment of the conventional epitaxial layer deposition temperatures and oxygen concentrations implicitly and/or explicitly taught in Wijaranakula, as explained by Wolf, in the semiconductor silicon-wafer making process of Wijaranakula would have been obvious to one of ordinary skill in the art. ***In re Peterson***, 315 F.3d 1325, 1329, 65 USPQ2d 1379, 1382 (Fed. Cir. 2003)("In cases involving overlapping ranges, we and our predecessor court have consistently held that even a slight

overlap in range establishes a ***prima facie*** case of obviousness."). This is especially true in this case since both Wijaranakula and Wolf recognize that the oxygen content and the epitaxial layer deposition temperature are result effective variables as indicated above. ***See In re Boesch***, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980)("[Discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art."); ***In re Aller***, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955)("[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."). Moreover, the fact that the epitaxial layer taught by Wijaranakula contains no nucleation sites or nuclei to form microdefects as indicated ***supra*** evinces that it is necessarily deposited at the conventional deposition temperature of greater than 1000° C. Compare the appellant's admission at page 9 of the Brief and Wijaranakula, column 2, lines 1-7, with Wijaranakula, column 3, lines 16-17.

The appellant separately argues that the substrate resistivity recited in claims 10 through 13 is not taught or suggested by the applied prior art references. See the Brief, pages 10 - 11. We do not agree.

As indicated ***supra***, the silicon substrate taught by Wijaranakula is preferably made by a Czochralski process. According to Wijaranakula (column 4, lines 24 and 35-38), the preferred silicon substrate is doped with less than 300 ppma, preferably approximately $3x10^{18}$ atoms/cm^3 of boron. Wolf at page 27, Table 2, indicates that the boron doped Czochralski silicon substrate taught by Wijaranakula has a substrate resistivity in the range of 0.005 to 50 ohm-cm which embraces the claimed substrate resistivity range. Wolf further explains that "[t]he resistivity is related to the doping density." See page 27. Figure 22 at page 28 of Wolf appears to show that at the concentration of a boron dopant preferred by Wijarankula, the substrate resistivity is within the claimed range. Thus, from our perspective, Wijaranakula either teaches or would have suggested employing a silicon substrate having the claimed resistivity as explained by Wolf. ***Peterson***, 315 F.3d at 1329, 65 USPQ2d at 1382; ***In re Malagari***, 499 F.2d 1297, 1303, 182 USPQ 549, 553 (CCPA 1974).

Thus, having considered the totality of record, including due consideration of all of the arguments proffered by both the examiner and the appellant, we determine that the examiner has established a ***prima facie*** case of obviousness, which has not been

sufficiently rebutted by the appellant. Accordingly, we affirm the examiner's decision rejecting claims 6 through 21 under Section 103(a).

CONCLUSION

In view of the foregoing, we affirm the examiner's decision rejecting all of the claims on appeal under Section 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

EDWARD C. KIMLIN)
Administrative Patent Judge)
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CHUNG K. PAK) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
PETER F. KRATZ)
Administrative Patent Judge)

CKP:TF

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ARENT, FOX, KINTNER, PLOTKIN & KAHN
SUITE 600
1050 CONNECTICUT AVENUE, N.W.
WASHINGTON, DC 20036-5339